

CLAIMS

What is claimed is:

- 1 1. A circuit comprising:
2 a multiplexer;
3 a space control register coupled to control the multiplexer;
4 a latch coupled to receive a signal from the multiplexer;
5 a control circuit coupled to control the latch, the control circuit to select one or
6 more bits from a stream of bits output by the multiplexer;
- 1 2. The circuit of claim 1 wherein the multiplexer comprises a plurality of
2 multiplexers.
- 1 3. The circuit of claim 2 wherein the plurality of multiplexers comprise first,
2 second, third, fourth and fifth multiplexers.
- 1 4. The circuit of claim 3 wherein the first, second, third and fourth
2 multiplexers are 8:1 multiplexers.
- 1 5. The circuit of claim 3 wherein the fifth multiplexer comprises a 6:1
2 multiplexer coupled to receive an output from the first multiplexer, an output from the
3 second multiplexer, an output from the third multiplexer, an output from the fourth
4 multiplexer, a logical "one", and a logical "zero".

1 6. The circuit of claim 1 wherein the space control register programmably
2 stores a value indicating a selected bit from a plurality of bits.

1 7. The circuit of claim 1 wherein the control circuit comprises:
2 a time control register to store a value indicating a selected bit from a sequence of
3 bits;
4 a counter to count bits in the sequence of bits from a predetermined bit;
5 a comparator coupled to the time control register and to the counter to generate a
6 load signal when a value stored in the time control register and a value provided by the
7 counter are equal, the load signal to cause the latch to load a value output by the
8 multiplexer.

1 8. The circuit of claim 1 further comprising:
2 a second multiplexer coupled to receive a signal output by the latch and to receive
3 a signal output by another circuit; and
4 a second control circuit to control the second multiplexer.

1 9. The circuit of claim 8 further comprising second latch coupled to receive a
2 signal output by the second multiplexer.

1 10. The circuit of claim 1, wherein the multiplexer receives logical values to
2 generate alarm signals.

1 11. A method comprising:
2 receiving multiple streams of bits; and
3 selecting one or more bits from a stream of bits based, at least in part, on a space
4 control register value and a time control register value.

1 12. The method of claim 11 wherein the space control register indicates a
2 selected stream of data from a plurality of streams of data.

1 13. The method of claim 12, wherein the space control register is
2 programmable.

1 14. The method of claim 11, wherein the time control register indicates one or
2 more bits from a selected stream of data.

1 15. The method of claim 14, wherein the time control register is
2 programmable.